UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/011,863	11/12/2001	Damoder Reddy	SMA-001.1D	6005

7590 01/13/2004

RONALD CRAIG FISH
RONALD CRAIG FISH, A LAW CORPORATION
POST OFFICE BOX 2258
MORGAN HILL, CA 95038

EXAMINER	
NGUYEN, KHIEM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 01/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/011,863	REDDY, DAMODER	
	Examiner	Art Unit	
	Khiem D Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 October 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 April 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 20, 2003 has been entered. A new rejection is made as set forth in this Office Action. Claims (1-4) are pending in the application.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-4 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The term "low-temperature" as recited in independent claims 1-4 has no patentable weight because it cannot be determined by any reasonable degree as to evaluate the term "low".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tuttle et al. (U.S. Patent 6,375,780) in view of Charles Lynch (Practical Handbook of Materials Science, pages 281-282 and 292-293).

In re claim 1, **Tuttle** discloses an integrated circuit structure comprising (See **FIGS. 1A-15** and related text): a plastic or glass or plastic laminated to glass substrate **(FIG. 5A, 68)** and a layer of substrate insulation comprised of silicon nitride formed on the substrate using low-temperature thin-film integrated circuit processing techniques performed using temperatures and materials which will not damage the substrate, the layer formed so as to have a thickness such that little or no differential strain between the substrate and the layer of substrate insulation occurs at any temperature in the normal operating temperature range of the device (col. 13, lines 19-28);

an antenna conductor **(FIG. 9, (154, 156))**, which is bonded onto, integrated onto or printed onto the layer of substrate insulation (col. 13, lines 39-40) and having two conductive pads or other conductive terminal areas where electrical connection to the antenna is capable of being made (col. 12, lines 8-11);

an antenna insulation layer **(FIG. 9: 158)** formed over the antenna using low-temperature, thin-film integrated circuit fabrication techniques using temperature and materials which will not damage previously formed structures of the device, the antenna insulation layer formed so as to have vias or contact holes over the conductive terminal area of the antenna conductor (col. 11, lines 3-9 and **FIGS. 7-9**);

a layer of silicon deposited on the antenna insulation layer using thin-film, low-temperature integrated circuit processing techniques using temperature and materials which will not damage previously formed structures of the device (col. 11, lines 3-9 and **FIG. 9**);

an integrated circuit comprising an RFID tag or smart card transceiver and processor and memory **(FIG. 9, 150)** integrated in the layer of silicon using low-temperature, thin-film integrated circuit processing techniques carried out at temperatures and using materials which will not damage previously formed structures of the device and formed so as to have RF input/output terminals which are electrically coupled to the conductive terminal areas of the antenna (col. 11, lines 3-9 and **FIGS. 7-9**).

Tuttle does not explicitly disclose wherein the layer formed so as to have thickness given the Young's Modulus and type of material of the layer of insulation and the Young's Modulus, thickness and type of material of the substrate.

However, all the materials have a Young's Modulus coefficient (**Charles Lynch**, Practical Handbook of Materials Science, pages 281-282 and 292-293).

2. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tuttle et al. (U.S. Patent 6,375,780) in view of Charles Lynch (Practical Handbook of Materials Science, pages 281-282 and 292-293).

In re claim 2, **Tuttle** discloses an integrated circuit structure comprising (See **FIGS. 1A-15** and related text): a plastic or glass or plastic laminated to glass substrate **(FIG. 5A, 68)** and a layer of substrate insulation comprised of silicon nitride formed on the substrate using low-temperature, thin-film integrated circuit processing techniques

performed using temperatures and materials which will not damage the substrate, the layer of substrate insulation formed so as to have a thickness such that little or no differential strain between the substrate and the layer of substrate insulation occurs at any temperature in the normal operating temperature range of the device (col. 13, lines 19-28);

a layer of silicon deposited on layer of substrate insulation using thin-film, low-temperature integrated circuit processing techniques using temperature and materials which will not damage previously formed structures of the device (col. 11, lines 3-9 and **FIG. 9**);

an integrated circuit comprising an RFID tag or smart card transceiver having antenna contacts and a processor and a memory **(FIG. 9, 150)** integrated in the layer of silicon using low-temperature, thin-film integrated circuit fabrication techniques performed using temperatures and materials which will not damage previously formed structures of the device, the transceiver portion of the integrated circuit formed so as to have RF input/output terminals (col. 11, lines 3-9 and **FIGS. 7-9**);

an integrated circuit insulating layer **(FIG. 9: 158)** formed over the integrated circuit using low-temperature, thin-film integrated circuit fabrication techniques using temperature and materials which will not damage previously formed structures of the device, and having contact holes formed therethrough to allow electrical connection to the RF input/output terminals of the transceiver (col. 11, lines 3-9 and **FIGS. 7-9**);

an antenna conductor **(FIG. 9, (154, 156))**, which is bonded onto, integrated onto or printed onto the integrated circuit insulating layer covering the transceiver so as to make electrical connection with the RF input/output terminals of the transceiver.

Tuttle does not explicitly disclose wherein the layer of substrate insulation formed so as to have thickness, given the Young's Modulus and type of material of the substrate insulation layer and the Young's Modulus, thickness and type of material of the substrate.

However, all the materials have a Young's Modulus coefficient (**Charles Lynch**, Practical Handbook of Materials Science, pages 281-282 and 292-293).

3. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tuttle et al. (U.S. Patent 6,375,780) in view of Charles Lynch (Practical Handbook of Materials Science, pages 281-282 and 292-293).

In re claim 3, **Tuttle** discloses an integrated circuit structure comprising (See **FIGS. 1A-15** and related text): a first plastic or glass or plastic laminated to glass substrate **(FIG. 5A, 68)** and a substrate insulation layer of silicon nitride formed on the substrate using integrated circuit processing techniques having temperatures and materials which will not damage the substrate, the substrate insulation layer formed so as to have a thickness selected such that little or no differential strain between the substrate and the substrate insulation layer occurs at any temperature in the normal operating temperature range of the device (col. 13, lines 19-28);

an antenna conductor **(FIG. 9, (154, 156))**, which is bonded onto, integrated onto or printed onto the substrate insulation layer (col. 13, lines 39-40) and having two

conductive pads or other conductive terminal areas where electrical connection to the antenna is capable of being made (col. 12, lines 8-11).

Tuttle does not explicitly disclose wherein the substrate insulation layer formed so as to have a thickness selected given the Young's Modulus of the material of the substrate insulation layer.

However, all the materials have a Young's Modulus coefficient (**Charles Lynch**, Practical Handbook of Materials Science, pages 281-282 and 292-293).

Tuttle discloses in (col. 11, lines 3-9 and **FIG. 9**) an RFID tag or smart card transceiver integrated circuit **150** using semiconductor processing techniques integrated on the substrate so as to have RF input/output terminals which are electrically coupled to the terminal areas of the antenna but does not explicitly disclose that an RFID tag or smart card transceiver integrated circuit integrated as one of a very large number of the integrated circuits on a large second plastic or glass substrate using flat panel display manufacturing equipment, the integrated circuit being cut from the second plastic or glass substrate and bonded or otherwise attached to the first plastic substrate and having RF input/output terminals wherein wires connected between the RF input/output terminals of the integrated circuit and the terminal areas of the antenna.

However, even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is

unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966.

4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tuttle et al. (U.S. Patent 6,375,780) in view of Charles Lynch (Practical Handbook of Materials Science, pages 281-282 and 292-293).

In re claim 4, **Tuttle** discloses a memory device comprising (See **FIGS. 1A-15** and related text): a plastic or glass or plastic laminated to glass substrate **(FIG. 5A, 68)**, a layer of substrate insulation comprised of silicon nitride formed on the substrate using low-temperature, thin-film integrated circuit processing techniques performed using temperatures and materials which will not damage said substrate, the layer formed so as to have a thickness, such that little or no differential strain between said substrate and said layer of substrate insulation occurs at any temperature in the normal operating temperature range of the device (col. 13, lines 19-28);

a layer of silicon deposited on the antenna insulation layer using thin-film, low-temperature integrated circuit processing techniques using temperatures and materials which will not damage previously formed structures of said device (col. 11, lines 3-9 and **FIG. 9**);

an EEPROM memory having a source, drain and channel region integrated in the layer of silicon and having a gate insulation layer formed over the channel region which is thin enough to allow tunnelling when programming voltages are applied, and having a gate, and having an intergate insulation layer formed over the gate, and having a control gate formed over the intergate insulation layer, all structures forming the EEPROM

memory formed using low-temperature, thin-film integrated circuit processing techniques carried out at temperatures and using materials which will not damage previously formed structures of the device (col. 2, lines 39-59 and **FIGS. 1-9**);

an EEPROM insulation layer **(FIG. 9: 158)** formed over the EEPROM memory using low- temperature, thin-film integrated circuit processing techniques carried out at temperatures and using materials which will not damage previously formed structures of the device, the insulation layer formed so as to have contact holes therein to allow electrical contact to the control gate and the source and drain regions of the memory (col. 11, lines 3-9 and **FIGS. 7-9**);

a contact metallization layer formed over the EEPROM insulation layer so as to make electrical contact with the control gate and the source and drain regions of the EEPROM memory **(FIGS. 1-9)**.

Tuttle does not explicitly disclose wherein the layer formed so as to have a thickness, given the Young's Modulus and type of material of the layer of insulation and the Young's Modulus, thickness and type of material of the substrate.

However, all the materials have a Young's Modulus coefficient (**Charles Lynch**, Practical Handbook of Materials Science, pages 281-282 and 292-293).

Response to Arguments

In response to Applicant's argument that Tuttle does not teach selecting a thickness for the barrier layer based upon its Young's modulus and the thickness and material and Young's modulus of the substrate so as the minimize differential strain between the substrate and the barrier layer, examiner respectfully disagree, Applicant is

directed to page 4, 2nd paragraph presented in this Office Action where the above limitation is addressed.

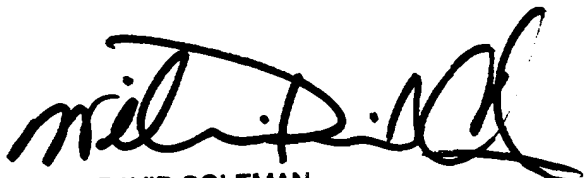
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (703) 306-0210. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

K.N.
January 8, 2004



W. DAVID COLEMAN
PRIMARY EXAMINER